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# **Finite State Machine**

### Introduction

This lab report details the exploration and practical demonstration of a D-type flip-flop circuit using the SN74HC74N integrated circuit. Building upon the foundational understanding of Finite State Machines.

### Methodology

The experiment involved constructing a D-type flip-flop circuit on a breadboard using the SN74HC74N IC, which houses two independent D flip-flops. The circuit incorporated various components including push-buttons for data input (D), preset (PR), and clear (CL) signals, LEDs to visualize the output states Q and Q'.

The experiment followed these key steps:

**Circuit Design and Implementation:** Following the pin configuration of the SN74HC74N IC, the D flipflop circuit was carefully constructed on a breadboard. This involved connecting the D, PR, CL, and clock inputs to the respective pins of the IC, and connecting the Q and Q' outputs to LEDs for visual indication.



**Truth Table Verification**: The experiment systematically tested the D flip-flop's behavior by applying different input combinations for D, PR, CL, and the clock signal. The observed output states (Q and Q') were then compared against the expected behavior according to the D flip-flop truth table.

Clock	INPUT			OUTPUT	
	PRESET	CLEAR	D	Q	Red
×1	HIGH	LOW	Х	1	0
×2	LOW	HIGH	Х	0	1
x	HIGH	HIGH	Х	1	1
HIGH	LOW	LOW	0	0	1
HIGH	LOW	LOW	1	1	0

Figure-1: Truth Table

# **Results and Discussion**

The experiment successfully verified the functionality of the D-type flip-flop. The observed output states for different input combinations aligned with the expected behavior outlined in the truth table.



Figure-2: Result of first row



Figure-3: Result of second row

## **Results and Discussion**

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## Conclusion

This lab experience provided valuable hands-on experience with D-type flip-flops, solidifying the understanding of their working principles and potential applications. By building and testing a D flip-flop circuit, the experiment effectively bridged theoretical knowledge with practical implementation, reinforcing key concepts related to sequential logic and FSM design.