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EE-102 - 01

23-24 SPRING

LAB 4: Arithmetic Logic Unit (ALU)

A) Purpose

This project aimed to design a basic Arithmetic Logic Unit (ALU) using VHDL for implementation on the BASYS 3 FPGA board. The ALU performs various mathematical and logical operations on 3-bit unsigned integers.

B) Methodology and Design Specifications

1. **Functionality Selection:** Eight functionalities were chosen for the ALU: addition, subtraction, left shift, OR, AND, XNOR and 2 comparison operation.
2. **Bit Width:** The design utilizes 3-bit unsigned numbers for inputs A and B and provides an output.
3. **Modular Design:** The VHDL code is structured in a modular fashion. There are two main 3 bitted inputs A and B. There is also selection input. The top-level module manages user selections and outputs the results based on the chosen operation. Eight sub-modules handle specific functionalities:
 - Adder: Performs 3-bit unsigned addition.
 - Subtractor: Executes 3-bit subtraction.
 - Shifter.: Implements a left shifter for 3-bit values.
 - OR gate: Defines a 3-bit OR gate.
 - AND gate: Defines a 3-bit AND gate.
 - XNOR gate: Defines a 3-bit XNOR gate.
 - comparator (circular and left): Compares two 3-bit unsigned numbers.

MODE	3-Bit	FUNCTION
Adder	000	A+B
Subtractor	001	A-B
Comparator	010	A<B , A>B
Shift (Circular)	011	
Shit (Left)	100	
XNOR gate	101	A XNOR B
NAND gate	110	A NAND B
NOR gate	111	A NOR B

4. Testing and Verification: A test bench was created to verify the functionality of each operation. The waveform was recorded for analysis.
5. Bitstream Generation: A constraint file was generated, and the VHDL code was synthesized into a bitstream for FPGA implementation.
6. Hardware Implementation: The bitstream was downloaded to the BASYS 3 board for hardware testing using switches for input and LEDs for output visualization.

C)Results

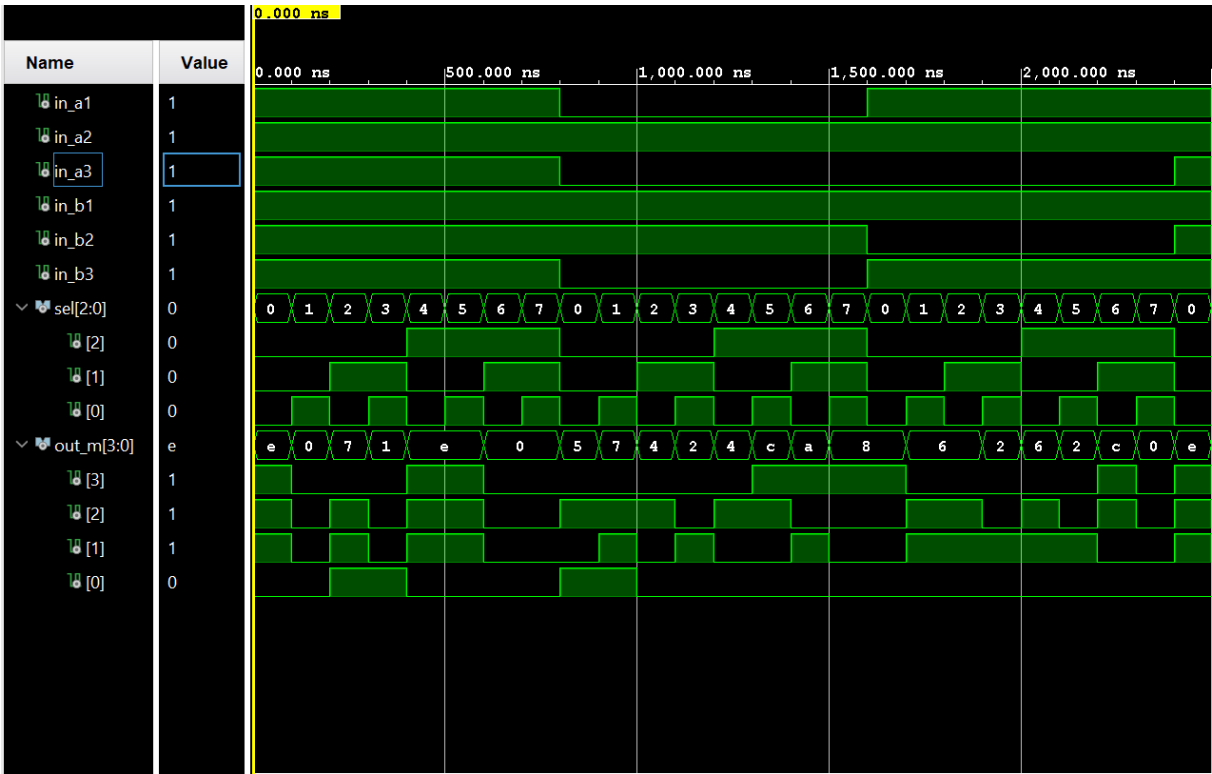


Figure.1 Test Bench Simulation

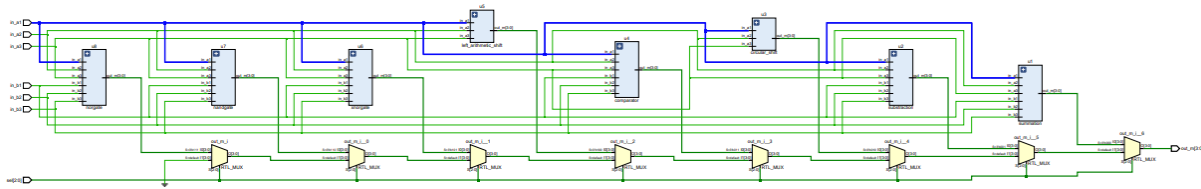


Figure.2 RTL schematic

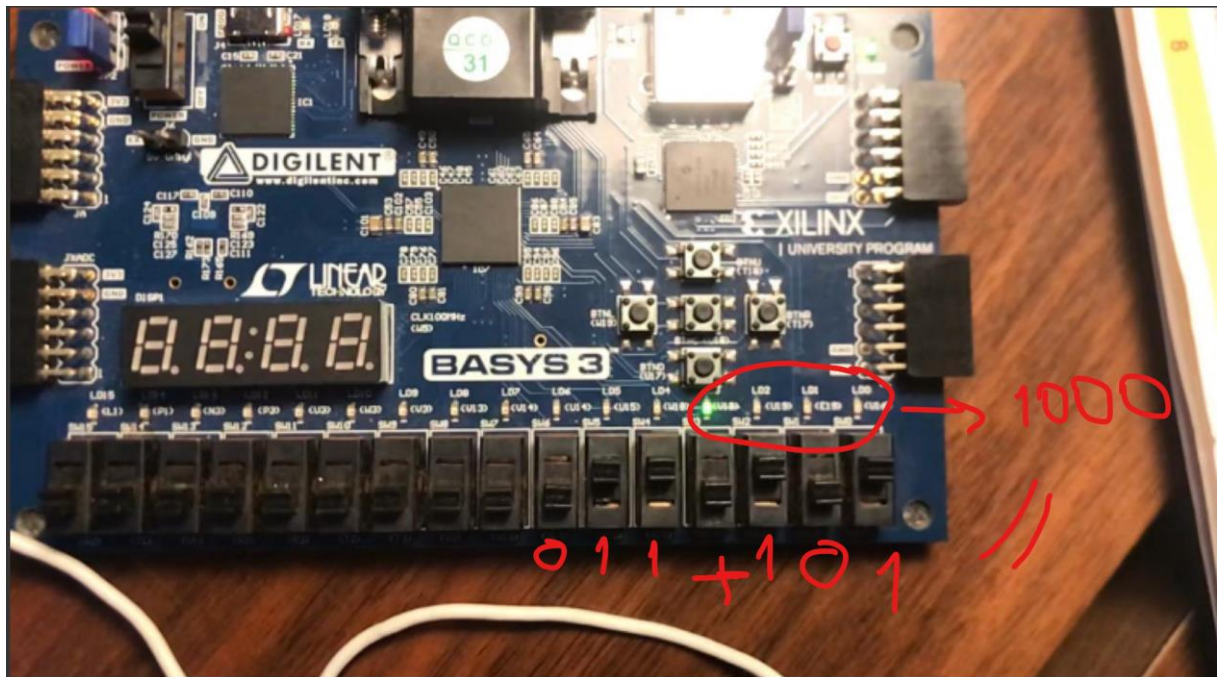


Figure.3 Adder

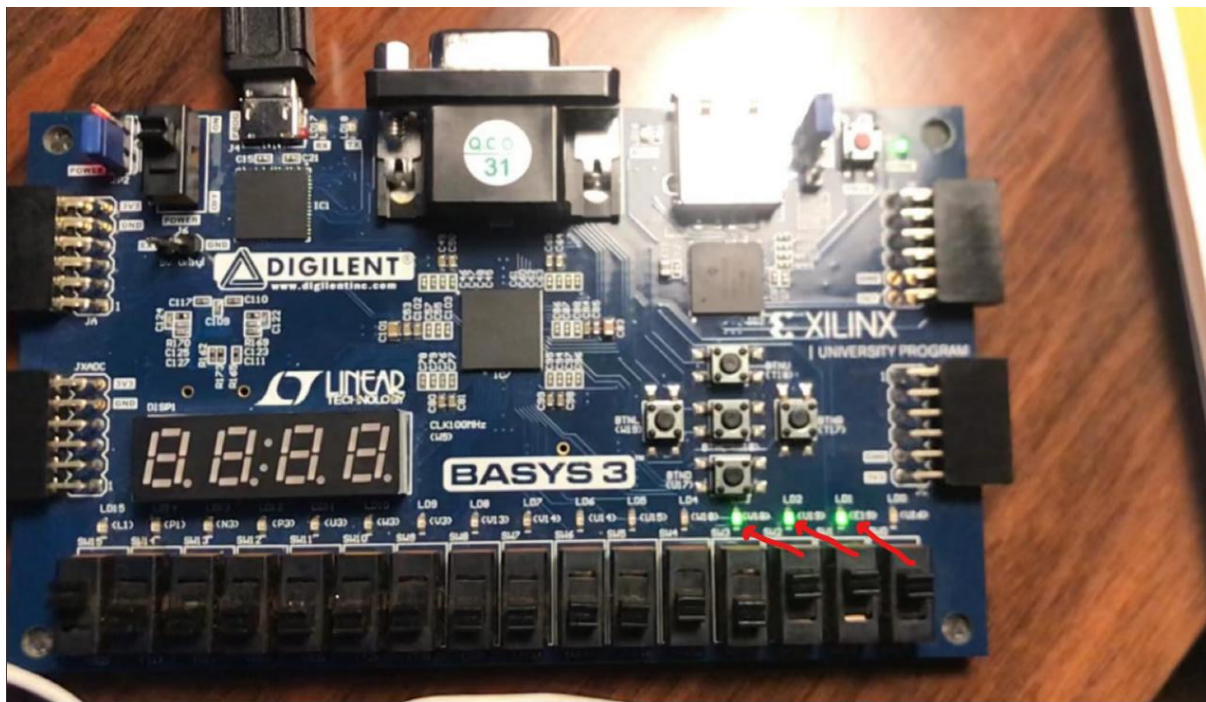


Figure.4 Left Shifter

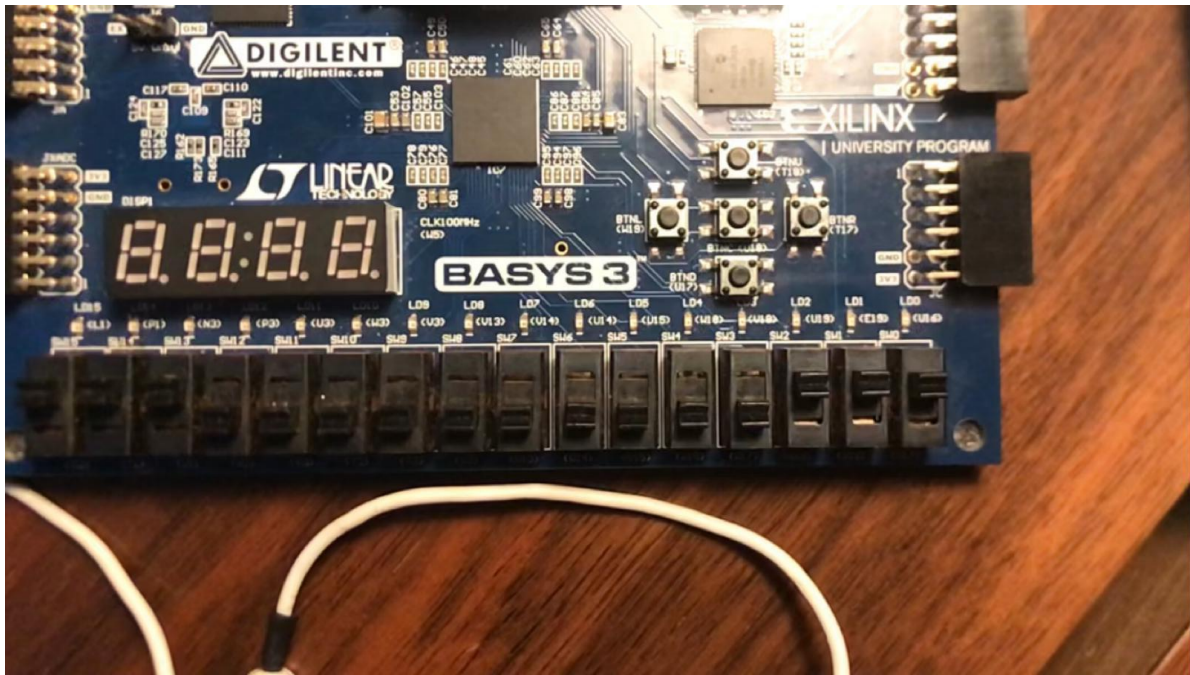


Figure.5 XOR Gate

D)Conclusion

This project successfully implemented a basic ALU with eight functionalities on the BASYS 3 board using VHDL. The design demonstrates a modular approach and showcases the use of various logic gates and arithmetic operations on 3-bit unsigned integers. The project highlights good practices for addressing design challenges like driver errors and conditional assignments in VHDL.