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EE-102 - 01

23-24 SPRING

LAB 3: Combinational Logic Circuit

A) Purpose

The main goal of this lab is to demonstrate our theoretical circuit design in practice on a breadboard. There are several additional objectives:

1. Learning to read and work according to datasheets:

   -Understanding how to use 74HC(T) 163 ICs in any mode (including count mode in this case)

   -Learning how to use HC08 (AND gate) and HC32 (OR gate) logic gates and how to connect them to other equipment

   -Grasping the function of a counter

2. Designing a logic circuit:

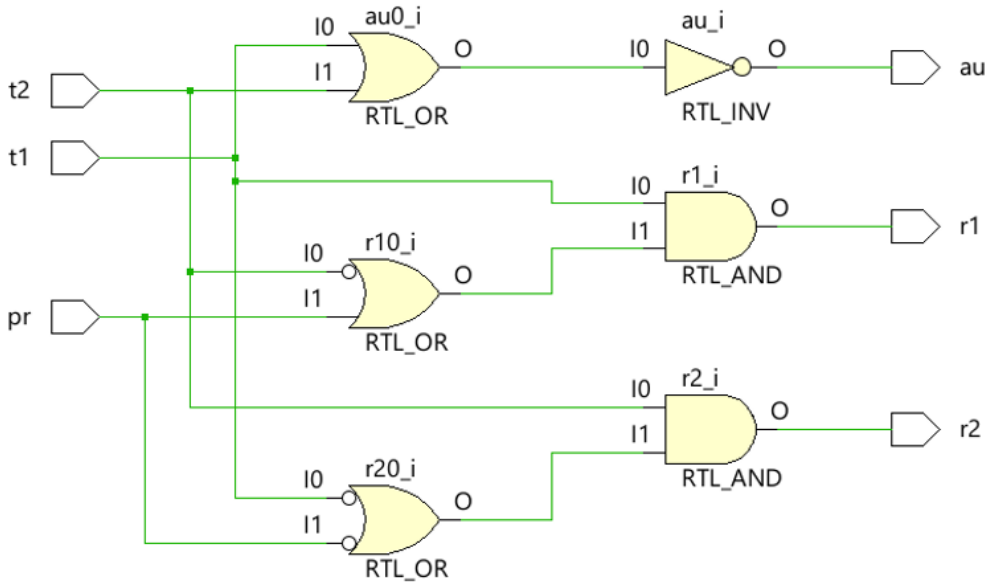
   -Learning how to translate a theoretical function into a practical circuit

   -Understanding basic gates (OR and AND gates)

   -Developing circuit design skills

B)Methodology

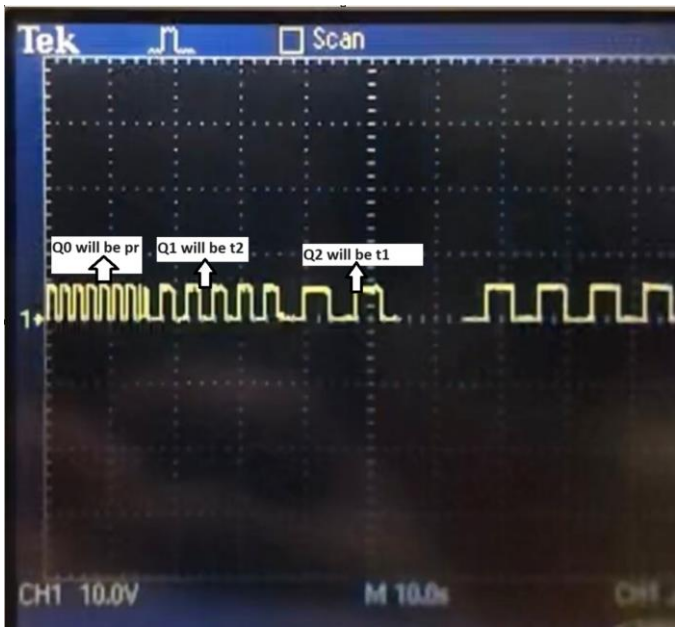
1-First, we need a circuit design to implement on a breadboard. I obtained one from a friend since I encountered difficulties with my previous lab design. This wasn't an issue, as the lab manual allows for designing a new circuit. Following that, I constructed a truth table for the chosen circuit design.



t_1	t_2	pr	au	r_1	r_2
0	0	0	1	0	0
0	0	1	1	0	0
0	1	0	0	0	1
0	1	1	0	0	1
1	0	0	0	1	0
1	0	1	0	1	0
1	1	0	0	0	1
1	1	1	0	1	0

2- Second, I studied the datasheet of the 74 HC(T) 163. This was a very important step, as almost every part of this lab involved using this IC. For example, I needed to use the count mode of the IC, and all the necessary information for operating it in this mode was found in the datasheet.

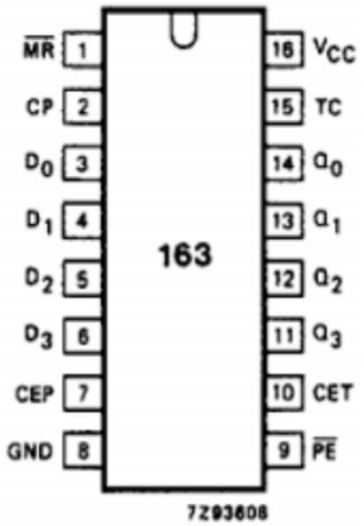
3-Then, I tested legs of the IC (74 HCT163) to determine if it works or not. The legs; Q_0, Q_1 and Q_2 was working properly. According to truth table, I chose Q_0 to pr, Q_1 to t2 and Q_2 to t1.



4-

CP IS CONNECTED TO RED PROBE OF THE SIGNAL GENERATOR. THE BLACK PROBE OF THE SIGNAL GENERATOR SHOULD BE CONNECTED TO GENERAL GND

GND TO GENERAL GND



MR
CEP
VCC
CET
PE
THESE ALL CONNECTED TO 5V

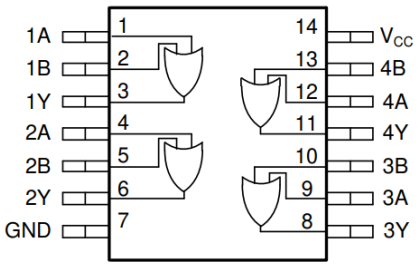
Q0-pr
Q1-t2
Q2-t1

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
reset (clear)	l	↑	X	X	X	X	L	L
parallel load	h h	↑ ↑	X X	X X	l l	l h	L H	L (1)
count	h	↑	h	h	h	X	count	(1)
hold (do nothing)	h h	X X	l X	X l	h h	X X	q_n q_n	(1) L

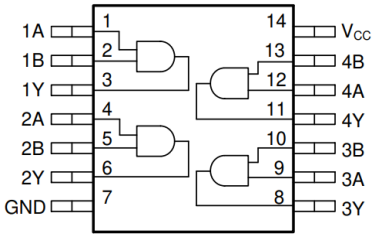
Using jumper cables, connect the MR, CEP, PE, CET, and V_{cc} pins to 5V. Connect the GND pin to ground. Some pins, like the D pins, are not needed for this mode. Connect the CP pin to the positive probe of the signal generator, which should output square waves, preferably between 1 and 3 Hz. Connect the negative probe of the signal generator to ground. Ignore any unused pins.

5. Based on the truth table and my circuit design, I simulated the circuit on a breadboard using jumpers. I used AND, OR, and NOT gates for the simulation. Connect all V_{cc} legs to the positive terminal of the power supply (5V) and all GND legs to the negative terminal.

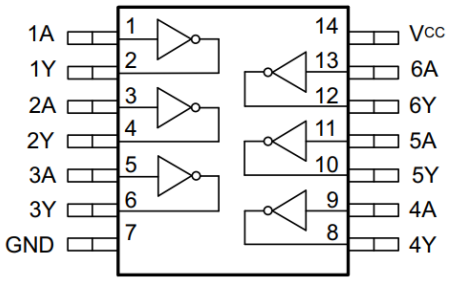
-HC08-AND gate:

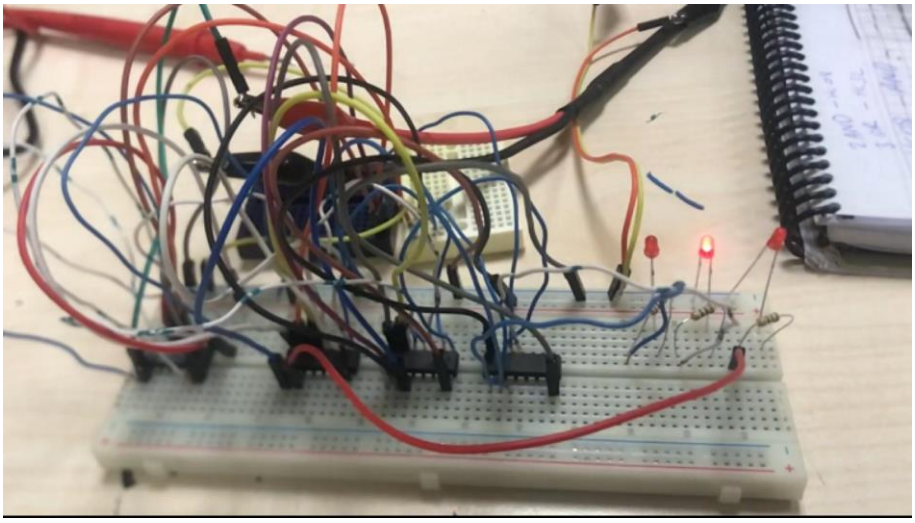


-HC32-OR gate:



-HC04-NOT GATE:



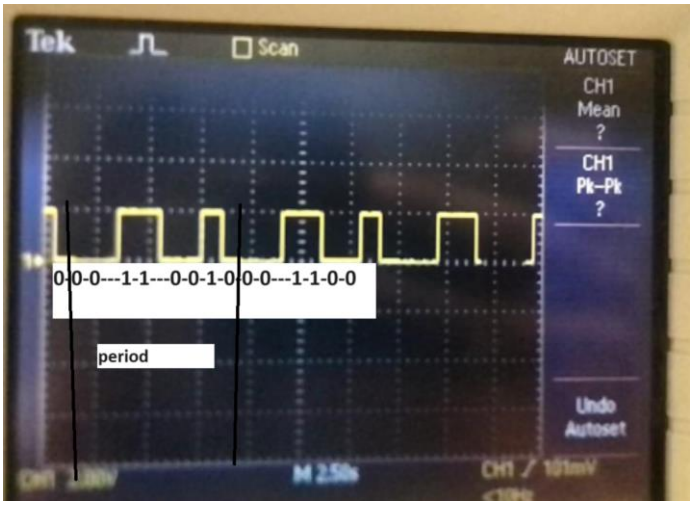


6- Finally, I added LEDs and resistors (560 Ω) to show my circiut is working according to my truth table.

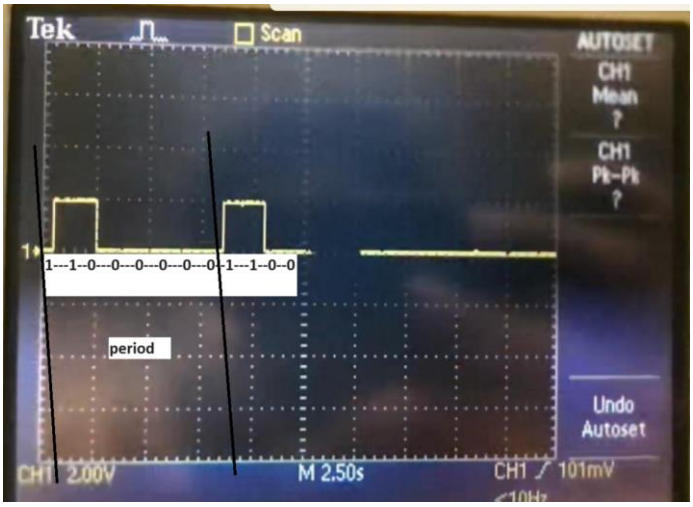
C)Results

Output-R1 results (matches with its truth table values):

Output-R2 results (matches with its truth table values):



Output-Au results (matches with its truth table values):



D)Conclusion

The goal of this lab is setting a logic circuit on the breadboard and simulate the truth table of the logic design and verify the results as a lighting LEDs. I could use my previous design but I could not. Studying datasheets was probably most important part. Moreover, datasheets are very helpful sources to design any circut.

However, there were many problems. For example, there are 4-5 ICs in the lab (74HCT163) and just one of them was working. There were also limited AND and OR gates.

In conclusion,
I learned
-reading and understanding datasheets,
-implementing therotical circuit design into practical
-AND, OR, NOT gates